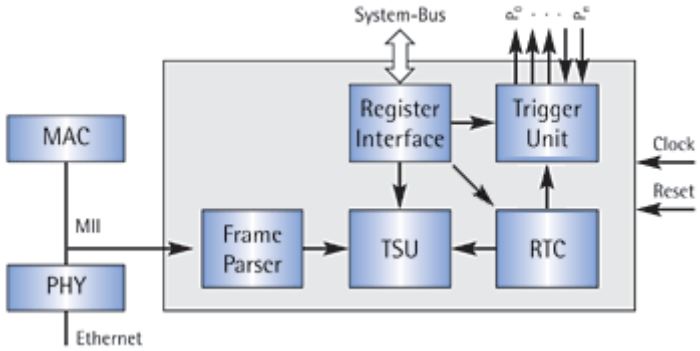
IEEE 1588 IP Core Module for FPGAs

For the clock adjustment between the local real-time clock and the master clock, it is necessary to provide the IEEE1588 telegrams with very accurate time stamps. If the used CPU has no IEEE1588 support, it is necessary to use software time stamping or to use an external IEEE1588 real time clock (RTC) with a time stamping unit (TSU). If the time stamp is generated by software, the clock synchronization is in the range from several 10 µs up to milliseconds.
If done in hardware (FPGA), the accuracy for the time stamp generation corresponds to the FPGA interal clock, which is depending on the frequency in the range of 20-50 ns. So a timer synchronization between master and slave clock in the double-digit nanosecond range is possible.



Using the trigger unit, changes of digital input signals can be captured chronological exactly via time stamps. In addition, it is possible to generate digital output signals, at this the starting time and the frequency can be specified exactly.

The IEEE1588 IP Core is intended for :

- Usage with a FPGA internal soft CPU like the Altera NIOS,
  running the IEEE1588 protocol software (IEEE1588 device as one chip solution)
- Usage with an external CPU running the IEEE1588 protocol
  software and application software

In both cases no special real-time requirements to the software environment are needed. It is completely sufficient to run the IEEE1588 protocol software cyclically, approx. every 10 - 100 ms. This results in a CPU load of less than 1 %.

Features

- Real time clock setting and adjustment via software
- Time stamping of external input signals via the trigger unit
- Triggering of external output signals based on
  configurable timers
- GMII interface for incoming and outgoing sync message detection (converters for MII and RMII are included in the scope of delivery)
- Support for IEEE1588 version 1 (IEEE1588-2002) and 2 (IEEE1588-2008)
- Time stamping of IPv4, IPv6 and IEEE 802.3 (layer 2) messages. Support can be activated in both the FPGA design and in the software.
- Standard address/data bus interface
- Buffer storage for time stamps and additional information for the message assignment incl. the possibility of interrupt generation
- Variable external clock frequencies possible
- Generation of a external PPS signal for clock accuracy measurements

Contents of Delivery

- Altera Mega Core (full license or OpenCore+)
- Encrypted VHDL code
- Device driver and demo application in C
- Reference design for IXXAT's Industrial Ethernet Module
- Manual
- Quick start guide
- 45 days technical support from date of delivery

Technical Data

- Number of logic elements (Altera): approximately 2000
- Accuracy:
  +/- 150 ns (external clock with 50 MHz)
  +/- 75 ns (external clock with 80 MHz)
- Encrypted IP-Core for Altera FPGAs

IEEE 1588 PTP Protocol Software

The IEEE 1588 protocol software enables simple, rapid development of IEEE 1588 compliant devices based on the IEEE1588 IP Core.